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(21) International Application Number: PCT/US91/06627 (22) International Filing Date: 18 September 1991 (18.09.91) (30) Priority data: 588,930 27 September 1990 (27.09.90) US (71) Applicant: E.I. DU PONT DE NEMOURS AND COMPANY [US/US]; 1007 Market Street, Wilmington, DE 19898 (US). (72) Inventor: YOUNG, James, C. ; 28 Jarrell Farm Drive, Newark, DE 19711 (US). (74) Agents: MEDWICK, George, M. et al.; E.I. du Pont de Nemours and Company, Legal/Patent Records Center, 1007 Market Street, Wilmington, DE 19898 (US).		(81) Designated States: AT (European patent), BE (European patent), CA, CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent). Published <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>
(54) Title: THERMAL STRESS-RELIEVED COMPOSITE MICROELECTRONIC DEVICE (57) Abstract <p>A microelectronic package comprising a rigid substrate (1) having mounted thereon a component (3) having a plurality of sides and an electrically functional layer (9) adjacent to at least two sides of the component (3), the component (3) and the electrically functional layer (9) being spatially separated by a guard band (7), the volume of the substrate (1) underlying the guard band (7) having at least one region (13d) of reduced rigidity which permits the substrate (1) to dissipate mechanical stresses generated therein when the device is subjected to heating.</p>		

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⁺ Any designation of "SU" has effect in the Russian Federation. It is not yet known whether any such designation has effect in other States of the former Soviet Union.

**THERMAL STRESS-RELIEVED COMPOSITE
MICROELECTRONIC DEVICE**

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Field of Invention

The invention relates to composite microelectronic devices which are configured to reduce the thermally induced stresses in the device generated by ordinary operation.

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Background of Invention

To accomplish high functional density, high speed and highly reliable operation, microelectronic devices, such as VLSI (very large scale integration) silicon chips, are increasingly being combined with an interconnected multilayer structure on a substrate to form a compact composite microelectronic package.

A typical composite package is comprised of a ceramic substrate on which is mounted firmly an integrated circuit (IC) chip. The IC chip is electrically interconnected to a plurality of conductive and dielectric layers surrounding the chip which are also firmly attached to the substrate, but spatially separated from the chip.

Figures 1 and 2a show a typical composite package with a chip wire-bonded across a narrow channel to interconnected multiple conductive and dielectric layers surrounding the chip, and both the chip and the multilayer structure are attached firmly to a common base substrate.

This type of package involves several materials with different coefficients of thermal expansion and moduli of elasticity. A difference between operating temperatures and the temperature at which the package was manufactured results in thermally induced stresses and deformations that affect the reliability. They are very difficult to eliminate due to the inherent mismatch in the coefficients of thermal expansion between the multilayer component, usually made of copper and polyimide, and the silicon chip.

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The conventional approach in this situation is to select a substrate material that produces the lowest stresses in both the chip and the multilayer component. But a complex thermomechanical interaction still exists through the substrate, since it is impossible to match the coefficients of thermal expansion for the three key package components, i.e., the chip, the multilayer and the substrate, all at once. The present invention provides an improved substrate design that reduces the mechanical interaction among the three.

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Summary of the Invention

The invention is directed to a microelectronic device comprising a rigid substrate having a component mounted thereon, the component having a plurality of sides and an electrically functional layer adjacent to at least two sides of the component and the electrically functional layer being separated by a guard band, the volume of the substrate underlying the guard band having one or more regions of reduced rigidity which permit the substrate to flex, thereby to dissipate mechanical stresses generated therein when the device is subjected to heating.

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Definition:

As used herein, the term "guard band" refers to the unoccupied surface area of a substrate which by virtue of physical spacing serves to isolate adjacent electrically functional elements mounted on the substrate.

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Brief Description of Drawings

The drawing consists of six figures. Figure 1 is an orthographic projection of a conventional composite microelectronic package. Figure 2a is a schematic section of a conventional composite microelectronic package and figures 2b through 2e are schematic sections of microelectronic packages which have been configured in accordance with the

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invention. Figure 3a is a graphical representation of the in-plane normal stresses of a conventional microelectronic package and 3b is a graphical representation of such stresses in a like microelectronic package which has been configured in accordance with the invention. Figure 4 is a bar chart which compares the in-plane thermal stresses of ungrooved and grooved substrates. Figure 5 is a bar chart which compares the in-plane thermal stresses of copper layers on both ungrooved and grooved substrates. Figure 6 is a bar chart which compares the in-plane thermal stresses of a silicon die mounted on both ungrooved and grooved substrates.

Prior Art

15 U.S. 3,325,882 and U.S. 3,428,866, Chiou et al

These divisional patents are directed to a packaging arrangement and method for interconnecting metal lands to a solid state device which is bonded to the floor of a cavity in the substrate so as to form a gap around the device to separate the device from the cavity walls. This is in contrast to the invention which uses a circumferential groove to decouple the stresses.

U.S. 4,374,457, Wiech et al

25 In this patent, Wiech provides a series of conductive filled grooves around the periphery of the cavity containing one or more semiconductor chips to form an electrical bus structure. In contrast with the invention multiple grooves are fabricated around the periphery of the cavity in the substrate and metallized.

U.S. 4,495,025 Haskell

35 The patent is directed to a photoresist process for forming grooves in semiconductor materials for the purpose of isolation of integrated circuits. The patent does not

disclose or suggest the function of grooves in substrates for any reason.

- 5 Bar-Cohen "Bonding Relations for Natural Convection Heat Transfer from Vertical Printed Circuit Boards" - Proceedings of the IEEE, Vol. 73, No. 9, September 1985.

10 This article suggests that vertical and horizontal grooves that are machined in the surface of plates with component-carrying printed wiring boards enhance the heat transfer characteristics of the assembly when the plates are spaced closely together. However, there is no mention made of thermal-mechanical coupling effects and how these can be neutralized by grooving substrates around each component bonded to the substrate.

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Detailed Description of the Invention

20 The invention is based upon fabricating the substrate in such a manner that the attached chip expands and contracts at a rate relatively independently of the expansion and contraction rates of the remaining interconnected package components that are also attached to the substrate.

25 The substrate in accordance with the present invention includes a small flexible substrate region of reduced rigidity having a finite surface area wherein the area occupies a substantial space beneath the guard band that separates the chip and the surrounding package components. This region of reduced rigidity is connected to two rigid substrate sections wherein one rigid section supports the chip and the other supports the remaining interconnected package components. The flexible section provides a forgivable mechanical linkage between the two rigid sections wherein the chip attached to one rigid section can expand and contract more or less independently, irrespective of the expansion and

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- 5 -

contraction of other package components attached to the other rigid section.

As a feature of the present invention, the small flexible section can be a flexible material (Fig. 2b) or a thin section (Fig. 2c-e) formed by continuous or discontinuous grooves. In the complete package, the thermally-induced stress and deformation in the chip caused by other package components, or vice versus, are extremely small so that the changes for chip or interconnects failures are reduced. Yet the complete substrate or package has the traditional exterior dimensional appearance and overall is still very rigid structurally so that it can be handled with traditional package assembly methods.

Turning now to the Drawing, Figures 1 and 2a illustrate the structure of a conventional composite microelectronic package consisting of an inert ceramic substrate 1 on which is firmly mounted an integrated circuit chip 3. The substrate can be made of such materials as AlN, SiC, Al₂O₃, Si, quartz, mullite, cordierite and gallium arsenide. The chip 3 is adhered to substrate 1 by means of an adhesive layer 5 which may be either inorganic and/or organic in nature. Typically, the adhesive layer, also known as the die-attach layer, is an organic thermoplastic or thermoset polymer such as those which are disclosed in EP 88104940.7, which is incorporated herein by reference. Surrounding the chip 3 is a dielectric layer 7 on which is mounted a series of conductive signal/power planes 9. The chip and dielectric layer 7 are separated by a guard plane and the chip 3 is connected electrically to the signal/power planes 9 by a series of fine conductive wires 11 which are typically made of gold or copper metal. The substrate 1 of Figure 1 has not been grooved or otherwise stress-relieved in accordance with the invention.

Figures 2b through 2e illustrate devices similar to that of Figures 1 and 2a, but differ in that each has a region

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of reduced rigidity to effect relief of the thermally induced stresses. In Figure 2b, the reduced rigidity region is comprised of a solid material 13b which is a more flexible solid than the rigid material of the remainder of the substrate. Figure 2c illustrates a package in accordance with the invention in which the region of reduced rigidity consists of a groove 13c cut into the top of the substrate and extending through about 80% of the substrate thickness. The groove can be continuous around the outer edges of the chip or it can be intermittent or discontinuous so long as the degree of stress relief is sufficient.

Figure 2d illustrates a package in accordance with the invention in which the region of reduced rigidity is comprised of two grooves 13d - one extending into the substrate from the top of the substrate and the other from the bottom of the substrate.

Figure 2e then illustrates a similar package in which the region of reduced rigidity is a single groove 13e extending into the substrate from the bottom of the substrate.

As mentioned above, the region or regions of reduced rigidity may extend continuously or discontinuously around the edges of the component so long as the region of reduced rigidity is sufficient to provide the desired degree of stress relief. In particular, it is preferred that the ratio of the modulus of elasticity of the substrate containing a region of reduced rigidity to the modulus of elasticity of the remainder of the substrate (Modulus Ratio) be less than 0.3. However, in order not to weaken the mechanical strength of the substrate excessively and make it too susceptible to breakage, the grooves or other configuration which constitute the regions of reduced rigidity should not extend through more than 80% of the thickness of the substrate. As used herein, the term "rigid substrate" refers to substrates having

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a modulus of elasticity before modification in accordance with the invention of at least 10Gpa.

Various configurations can be used for the regions of reduced rigidity. For example they can be round-bottomed or square-bottomed, they can have vertical or sloped sides. In general, the sides of the grooves need not correspond with the edge of the guard level and the outer edge of the chip. Nevertheless, such configurations are preferred. The overriding consideration is whether the reduced rigidity regions are of sufficient volume to render the Modulus Ratio below 0.3 and preferably below 0.1. Compliance with this criterion of Modulus Ratio can readily be determined by direct measurement of the moduli or it can be determined by computer modeling and analysis of the system.

The substrate can be made simply of a single base material such as those mentioned above or it can be a composite material consisting of a dispersion of particles or fibers in a matrix of a base material or base material mixture. Fibers can be used as a substrate filler in order to increase substrate strength. On the other hand, heat-conductive materials may be added as well in order to increase the ability of the substrate to conduct heat away from the microelectronic component. In general, substrates will be on the order of 40-80 mils in thickness of which 60 mils is typical. Thermally induced stresses on the substrate tend to be directly related to thickness, whereas stresses in the surrounding dielectric layers tend to be inversely related to substrate thickness.

Because the microelectronic chip is the source of heat which gives rise to the thermally induced mechanical stresses, it is preferred that the regions of reduced rigidity, which are most frequently grooves, be as close as possible to the chip but not underlying the chip. Typically, the grooves surrounding a component will not exceed about 10 mils in

width, which is the usual maximum width of the guard band in most composite packages. In addition the groove depth should not exceed about 80% of the substrate thickness. A substrate thickness of at least 10 mils should remain to avoid
5 excessively weakening the mechanical strength of the substrate.

When grooves are used to form the reduced rigidity region, they can be left open or they can be filled with a flexible material such as an elastomeric polymer or
10 other non-rigid filler material.

EXAMPLES

In Table 1 below, data are given which show the
15 maximum in-plane thermal stresses which are incurred in cooling from 170°C to 20°C. A single chip composite package comprising a copper ground layer and an IC chip mounted by means of polymeric die attach adhesive to an aluminum substrate. Because of the technical difficulty in measuring
20 actual in-plane stresses of such composite devices, the data were derived from finite element modeling of the deformation of each element based on the known TCE characteristics of each component. The dimensions of the components on which the modeling was based are as follows:

25 IC chip (1.27x1.27x0.051 cm)
Substrate (3.81x3.81x0.153cm)
Laminant (2 planes with 1.53x1.53 cm cavity)
Copper Layer (3.81x3.81x0.0036 cm)
Dielectric Layer (3.81x3.81x0.0025 cm)
30 Adhesive (3.81x3.81x0.0025 cm)

Groove dimensions are presented with the calculated maximum stresses shown in Table 1. In Table 1, data are presented showing the maximum in-plane thermal stresses incurred by the copper layer, the die attach adhesive
35 and the die itself when they are heated to 170°C and allowed

to cool to 20°C under ambient temperature conditions. In particular, maximum stress data are given for these components on an ungrooved substrate and substrates having three groove configurations and several groove sizes. These data show that all three groove configurations - single groove up, single groove down and double grooves up - were effective to reduce residual in-plane thermal stresses in all three components. However, the double groove up configuration was most effective and the single groove up configuration was significantly more effective than the single groove down configuration.

Table 1
In-Plane Residual Stresses of Grooved
and Ungrooved Substrates -
Effect of Groove Size and Configuration

Package Component	Copper Layer	Die Attach Adhesive	Die
Groove Configuration	Maximum Stress (MPa)		
Unmodified (modulus 9MPa)	213	56	759
Single Groove Up			
50/20 (1)	166	35	482
50/40	125	32	442
50/50	104	32	443
30/50	119	41	560
15/50	138	47	636
Single Groove Down			
15/50	169	51	689
50/50	165	51	687
Double Grooves Up			
15/50	117	32	447

(1) Width/depth in mils

The data given in the second column of the above Table with respect to thermal stresses in the copper layer can be observed graphically in Figure 4.

CLAIMS

1. A microelectronic device comprising a rigid substrate having a component mounted thereon, the component having
5 a plurality of sides and an electrically functional layer adjacent to at least two sides of the component, at least two sides of the component and the electrically functional layer being separated by a guard band, the volume of the substrate underlying the guard band having at least one region of
10 reduced rigidity which permits the substrate to flex, thereby to dissipate mechanical stresses generated therein when the device is subjected to heating.
2. The device of claim 1 in which the region of reduced
15 rigidity is continuous.
3. The device of claim 1 in which the ratio of the modulus of elasticity of the volume of the substrate containing a region of reduced rigidity to the modulus of elasticity of the
20 remainder of the substrate (Modulus Ratio) is less than 0.3.
4. The device of claim 3 in which the Modulus Ratio is less than 0.1.
- 25 5. The device of claim 1 in which the substrate has a predetermined thickness and the region of reduced rigidity has a predetermined depth which does not exceed 80% of the substrate thickness.
- 30 6. The device of claim 1 in which the modulus of elasticity of the unmodified substrate is at least 10 Gpa.
7. The device of claim 1 in which the region of reduced rigidity has a predetermined width which corresponds with
35 the width of the guard band.

8. The device of claim 7 in which the region of reduced rigidity extends from the upper surface into the volume of the substrate.
- 5 9. The device of claim 7 in which the region of reduced rigidity extends from the lower surface into the volume of the substrate.
- 10 10. The device of claim 1 having a plurality of reduced rigidity regions.
- 15 11. The device of claim 10 in which the regions of reduced rigidity extend from the upper surface into the volume of the substrate.
12. The device of claim 10 in which the regions of reduced rigidity alternately extend from the upper and lower surfaces into the volume of the substrate.
- 20 13. The device of claim 12 in which a first region of reduced rigidity extends from the upper surface into the volume of the substrate adjacent to the edge of the component.
- 25 14. The device of claim 1 in which the region of reduced rigidity is a groove.
15. The device of claim 14 in which the groove is continuous.
- 30 16. The device of claim 1 in which the region of reduced rigidity is comprised of a discontinuous series of grooves.
- 35 17. The device of claims 14 or 15 in which the grooves are filled with an inert non-rigid solid material.

18. The device of claim 1 in which the region of reduced rigidity is comprised of non-rigid material which is an integral part of the substrate.
- 5 19. The device of claim 1 in which the substrate is a composite layer of particles dispersed in a rigid solid matrix.
20. The device of claim 1 in which the substrate is a composite layer of fibers dispersed in a rigid solid matrix.
- 10 21. The device of claim 1 in which the substrate is comprised of ceramic solid material selected from AlN, SiC, Al₂O₃, silicon, quartz, mullite, cordierite and gallium arsenide.
- 15 22. The device of claim 1 in which the substrate is comprised of rigid polymeric material.
23. The device of claim 1 in which the component is an integrated circuit chip.
- 20 24. The device of claim 1 in which the electrically functional layer is a dielectric layer.
- 25 25. The device of claim 1 in which the substrate has a plurality of components mounted thereon.

1/6

PRIOR
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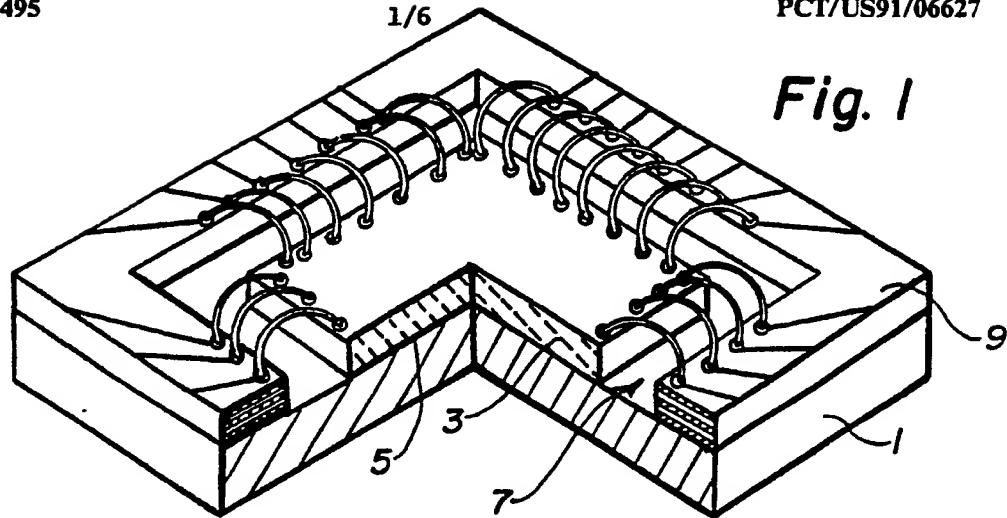


Fig. 1

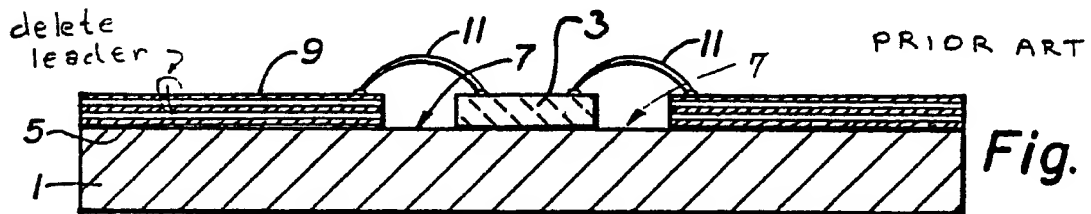


Fig. 2a

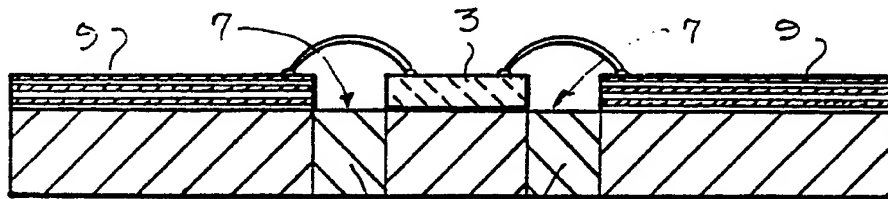


Fig. 2b

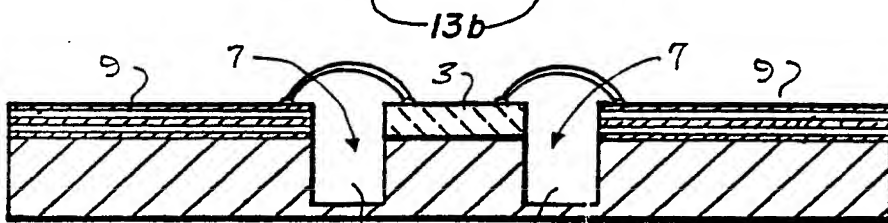


Fig. 2c

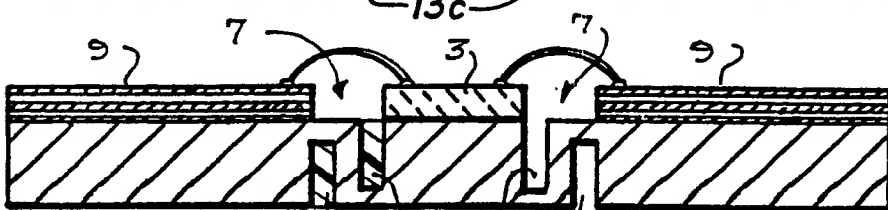


Fig. 2d

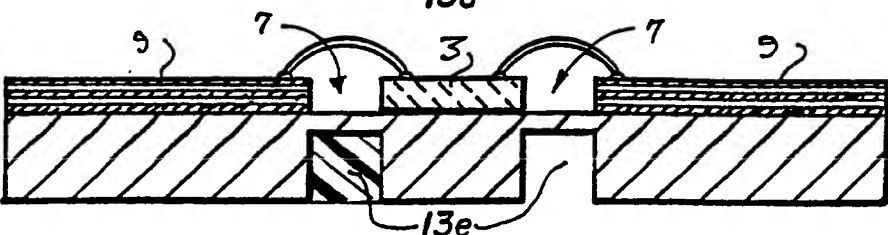
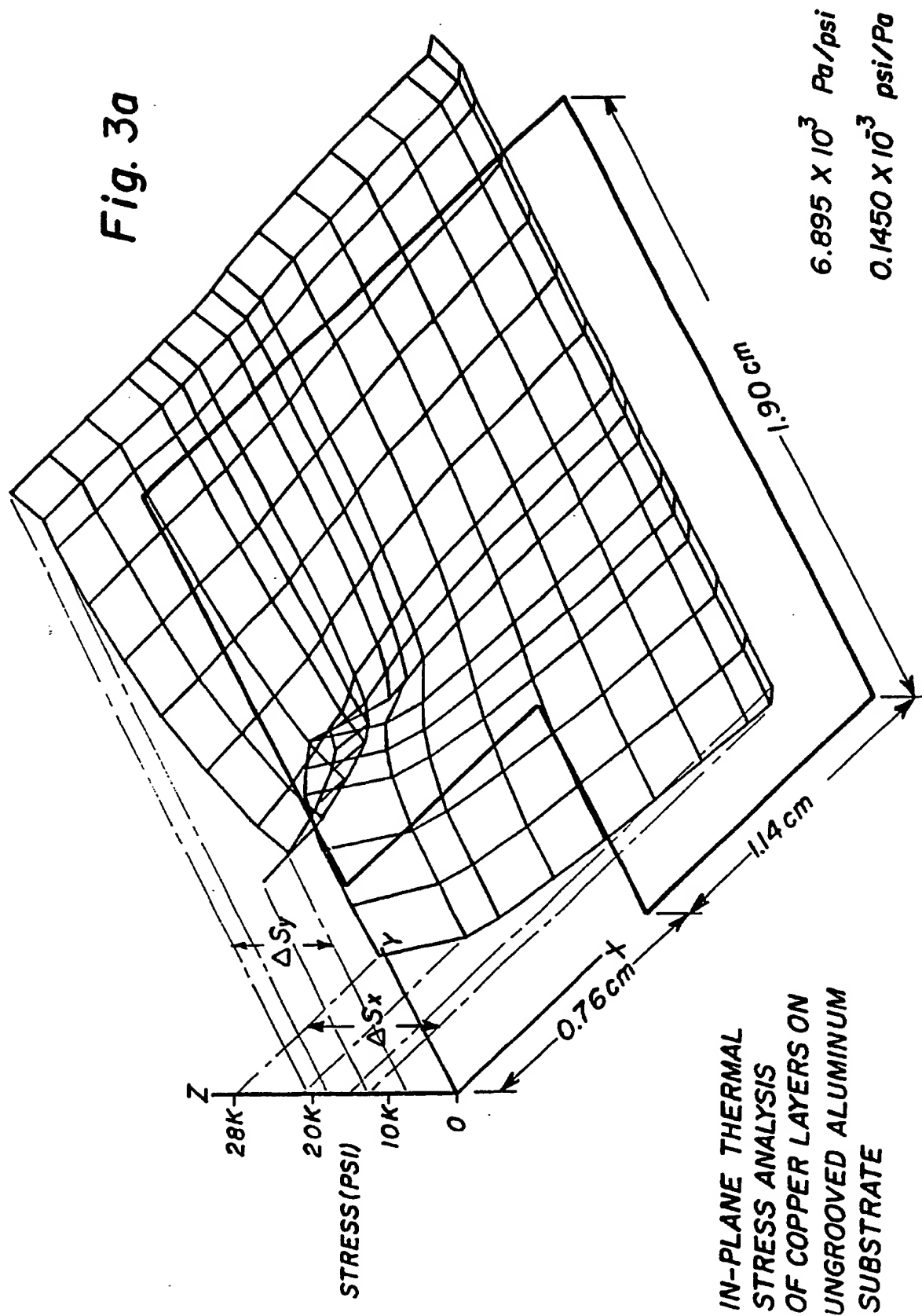


Fig. 2e

Fig. 3a



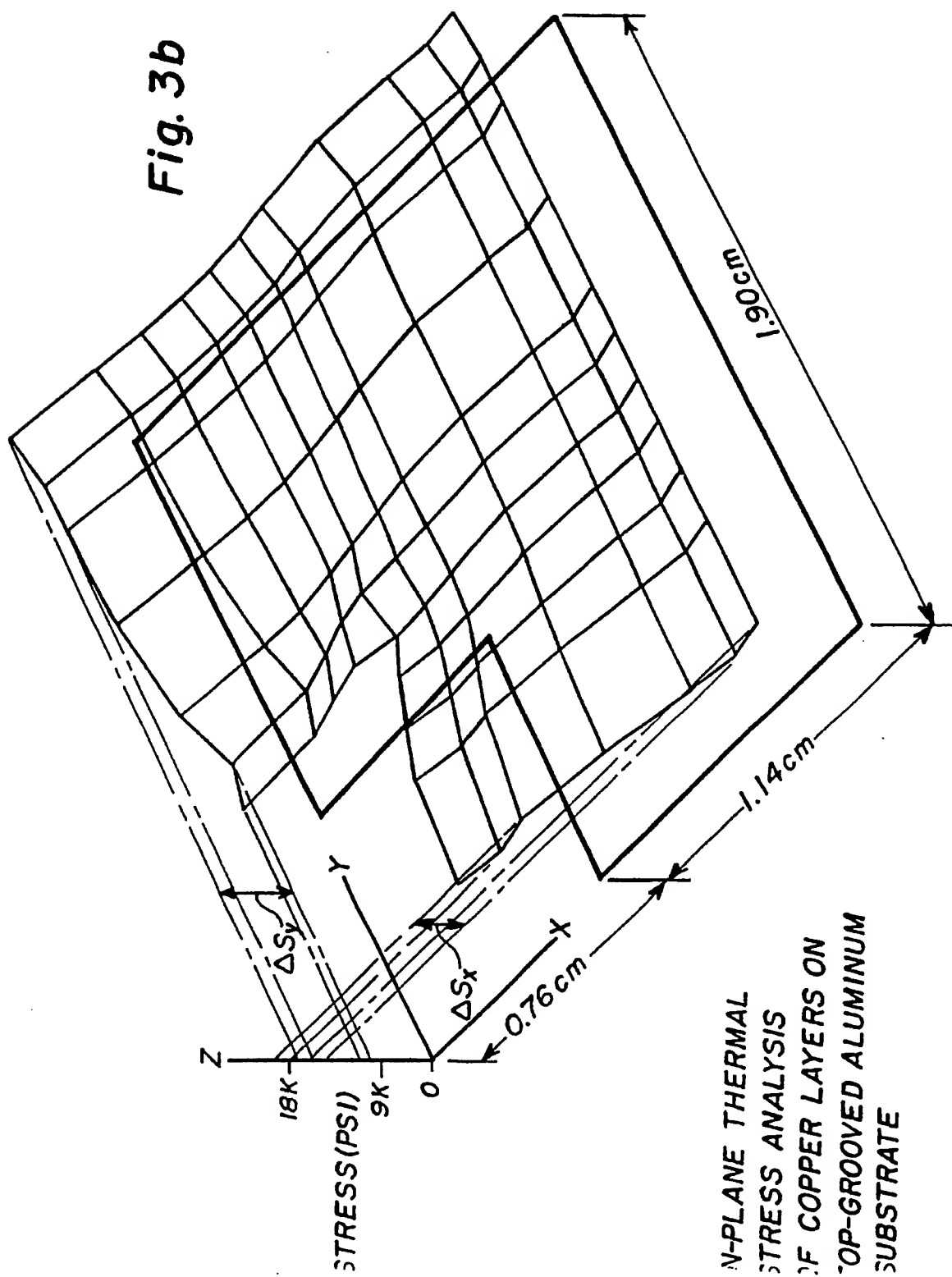
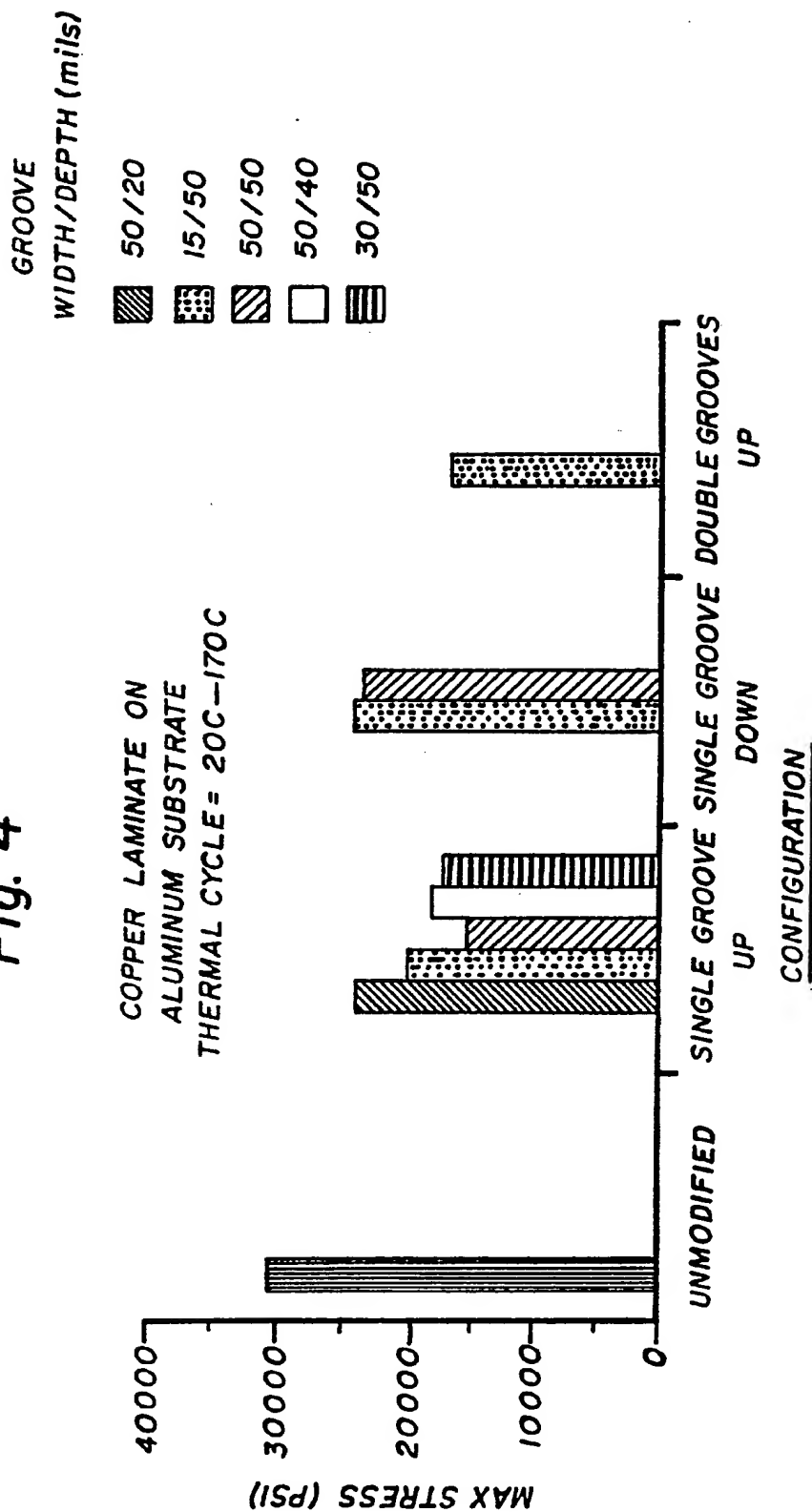
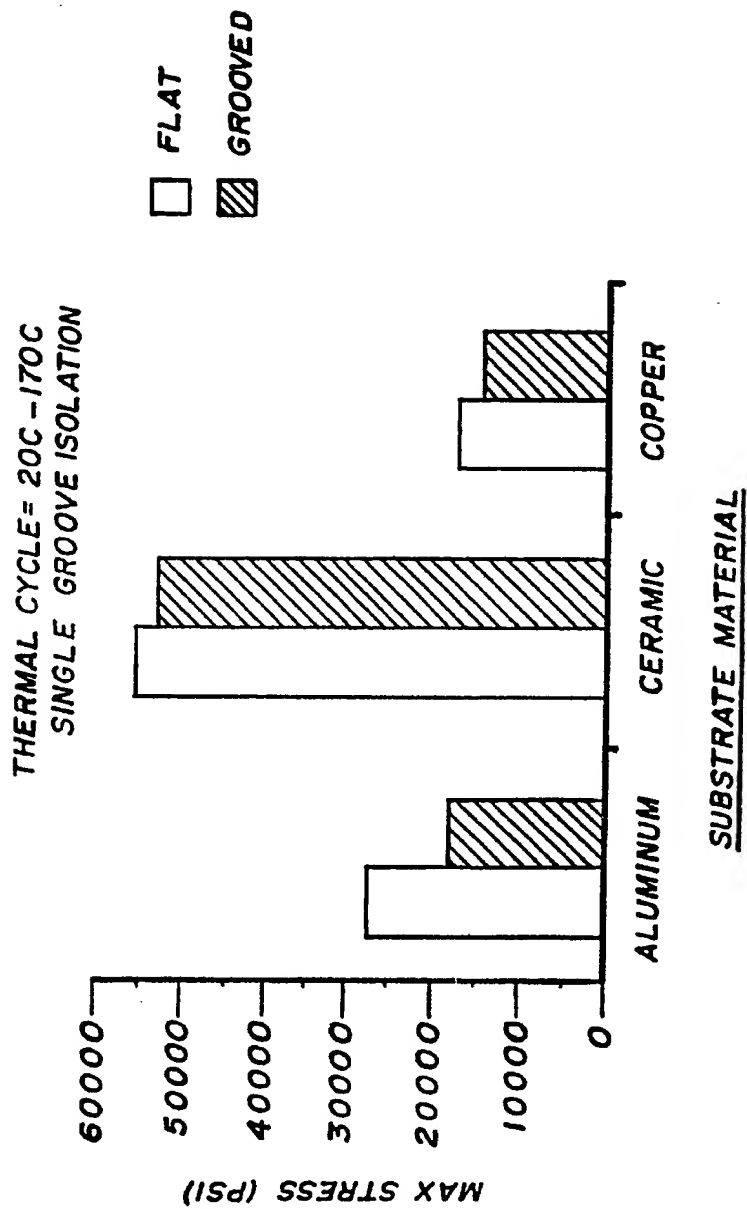


Fig. 4



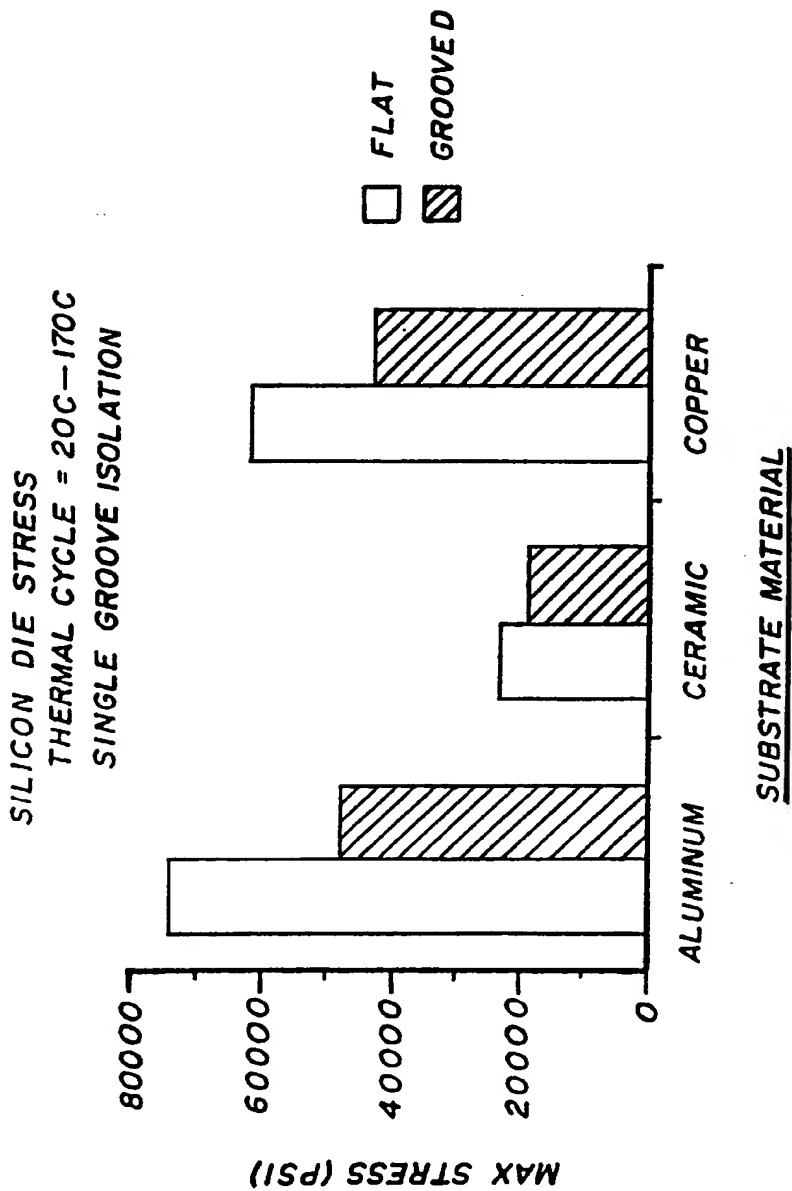
COMPARISON OF IN-PLANE THERMAL STRESSES
OF GROOVED AND UNGROOVED SUBSTRATES

Fig. 5



IN-PLANE THERMAL STRESS ANALYSIS OF COPPER LAYERS ON VARIOUS
SUBSTRATES: COMPARISON OF GROOVED AND UNGROOVED SUBSTRATES

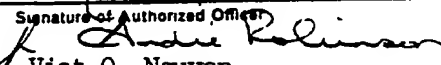
Fig. 6



IN-PLANE THERMAL STRESS ANALYSIS OF A SILICON DIE ON VARIOUS
SUBSTRATES: COMPARISON OF GROOVED AND UNGROOVED SUBSTRATES

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/06627

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC (5): H01L 23/12		
U.S.Cl.: 357/80, 84		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
Classification System	Classification Symbols	
U.S.	357/80, 84	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category ¹⁰	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
Y	US, A, 4,953,001 (KAISER, JR. ET AL.) 28 August 1990 (See Figure 1 and columns 1-2).	1-2,5,7-20 23, 25
Y	US, A, 4,563,697 (MIURA) 07 January 1986 (See Figure 3 and columns 1-3).	1-2,5,7-20 23, 25
<p>¹⁰ Special categories of cited documents:</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance: the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p>		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report	
20 February 1992	MAR 5, 1992	
International Searching Authority	Signature of Authorized Officer	
ISA/US	 Viet Q. Nguyen	

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET**V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE ¹**

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers _____, because they relate to subject matter ^{1,2} not required to be searched by this Authority, namely:

2. ☐ Claim numbers _____, because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out ^{1,3}, specifically:

3. ☐ Claim numbers _____, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING ²

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.
2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:
4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

- ☐ The additional search fees were accompanied by applicant's protest.
☐ No protest accompanied the payment of additional search fees.

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